WHAT IS CLAIMED IS:

1. A host messaging unit for allowing asynchronous retrieval of a command from a host processor, the host messaging unit comprising:

a memory storage device;

a read controller coupled to the memory storage device effective to asynchronously retrieve the command from the memory storage device; and

a write controller coupled to the memory storage device effective to asynchronously acknowledge the command retrieval, wherein the host processor is bypassed during both the command retrieval and the asynchronous acknowledgment of the command retrieval.

2. The host messaging unit of claim 1, wherein the read controller comprises:

a direct memory access read engine coupled to the memory storage device;

a read clock coupled to the direct memory access read engine to initiate the command retrieval from the memory storage device at predetermined intervals; and

a validator coupled to the direct memory access read engine to validate the command retrieved from the memory storage device.

3. The host messaging unit of claim 2, wherein the read clock allows programmable predetermined intervals.

4. The host messaging unit of claim 3, wherein the read clock restarts the predetermined interval after the command retrieval from the memory storage device.

5. The host messaging unit of claim 2, wherein the validator includes a comparator to indicate an invalid command when the command is zero valued.

6. The host messaging unit of claim 1, wherein the read controller comprises:

a direct memory access read engine coupled to the memory storage device; and

a busmaster command engine coupled to the direct memory access read engine to initiate the command retrieval from the memory storage when the busmaster command engine is signaled by the host processor.

7. The host messaging unit of claim 6, wherein the busmaster command engine comprises a register programmable by the host processor to indicate that the command is available to be retrieved from the memory storage device.

8. A peripheral component interconnect device comprising:

a device processor; and

a host messaging unit coupled to the device processor for facilitating communication between the device processor and an external device, the host messaging unit including:

a read controller coupled to the device processor effective to asynchronously read a data element from the external device; and

a write controller coupled to the device processor effective to asynchronously acknowledge the asynchronous read, wherein the device processor is bypassed during both the asynchronous read and the asynchronous acknowledgment of the asynchronous read.

9. The peripheral component interconnect device of claim 8, wherein the read controller comprises:

a direct memory access read engine coupled to read the data element from the external device;

a read clock coupled to the direct memory access read engine to initiate the data element retrieval from the external device at predetermined intervals; and

a validator coupled to the direct memory access read engine to validate the data element retrieved from the external device.

10. The peripheral component interconnect device of claim 9, wherein the read clock allows programmable predetermined intervals.

11. The peripheral component interconnect device of claim 10, wherein the read clock restarts the predetermined interval after the data element retrieval from the external device.

12. The peripheral component interconnect device of claim 9, wherein the validator includes a comparator to indicate an invalid data element when the data element is zero valued.

13. The peripheral component interconnect device of claim 8, wherein the read controller comprises:

a direct memory access read engine coupled to the external device; and

a busmaster command engine coupled to the direct memory access read engine to initiate the data element retrieval from the external device when the busmaster command engine is signaled by the external device.

14. The peripheral component interconnect device of claim 13, wherein the busmaster command engine comprises a register programmable by the external device to indicate that the data element is available to be retrieved from the external device.

15. In a computer system, a host processor coupled through a peripheral component interconnect bus to a peripheral component interconnect device, the peripheral component interconnect device comprising:

a host messaging unit for facilitating communication between the host processor and the peripheral component interconnect device, the host messaging unit including:

a read controller coupled to the host processor effective to asynchronously retrieve host processor commands from the host processor; and

a write controller coupled to the host processor effective to asynchronously acknowledge the command retrieval, wherein the host processor is bypassed during both the command retrieval and the asynchronous acknowledgment of the command retrieval.

16. The peripheral component interconnect device of claim 15, wherein the read controller comprises:

a direct memory access read engine coupled to the host processor;

a read clock coupled to the direct memory access read engine to initiate the command retrieval from the host processor at predetermined intervals; and

a validator coupled to the direct memory access read engine to validate the command retrieved from the host processor.

17. The peripheral component interconnect device of claim 16, wherein the read clock allows programmable predetermined intervals.

18. The peripheral component interconnect device of claim 17, wherein the read clock restarts the predetermined interval after the command retrieval from host processor.

19. The peripheral component interconnect device of claim 16, wherein the validator includes a comparator to indicate an invalid command when the command is zero valued.

20. The peripheral component interconnect device of claim 15, wherein the read controller comprises:

a direct memory access read engine coupled to the host processor; and

a busmaster command engine coupled to the direct memory access read engine to initiate the command retrieval from the host processor when the busmaster command engine is signaled by the host processor.

21. The peripheral component interconnect device of claim 20, wherein the busmaster command engine comprises a register programmable by the host processor to indicate that the command is available to be retrieved from the host processor.

22. A method of asynchronously servicing a peripheral component interconnect device comprising:

bypassing a host processor to access host commands from host memory;

using the host memory to signal the access of the host commands; and

providing status to the host processor after execution of the host commands.

23. The method of claim 22 wherein bypassing the host processor comprises:

allowing the host processor to write the host commands to the host memory; and

polling the host memory for valid host commands at predetermined intervals.

24. The method of claim 22 wherein using the host memory to signal the access of the host commands comprises writing zero valued data to the host memory containing the host commands.

25. The method of claim 22 wherein providing status to the host processor is interrupt driven.

26. The method of claim 25 wherein the interrupt driven status uses an interrupt pin to notify the host processor.

27. The method of claim 25 wherein the interrupt driven status uses message signaled interrupts to notify the host processor.

28. The method of claim 22 wherein bypassing the host processor comprises:

allowing the host processor to write the host commands to the host memory; and

interrupting the peripheral component interconnect device when the host commands are available in the host memory.

29. The method of claim 28 wherein interrupting the peripheral component interconnect device comprises writing a logic value to a register within the peripheral component interconnect device.

30. A method of reducing bus transfer overhead between a host processor and a peripheral component interconnect device processor comprising:

writing host processor commands to a memory storage device;

bypassing the peripheral component interconnect device processor to signal the existence of the host processor commands; and

bypassing the host processor to access the host processor commands from the memory storage device.

31. The method of claim 30 wherein bypassing the peripheral component interconnect device processor comprises using a host messaging unit to poll for host processor commands at predetermined intervals.

32. The method of claim 31 wherein bypassing the peripheral component interconnect device processor comprises interrupting the host messaging unit when the host commands are available in the memory storage device.

33. The method of claim 30 wherein bypassing the host processor comprises:

using a direct memory access read engine to retrieve host processor commands from the memory storage device; and

using a direct memory access write engine to signal the host processor that the host processor commands are retrieved.

34. An article of manufacture comprising a program storage medium readable by a computer, the medium tangibly embodying one or more programs of instructions executable by the computer to perform a method reducing bus transfer overhead between a host processor and a peripheral component interconnect device processor, the method comprising:

writing host processor commands to a memory storage device;

bypassing the peripheral component interconnect device processor to signal the existence of the host processor commands; and

bypassing the host processor to access the host processor commands from the memory storage device.

35. A peripheral component interconnect device comprising:

a device processing means; and

a host messaging means coupled to the device processing means for facilitating communication between the device processing means and an external device, the host messaging means including:

a read controlling means coupled to the device processing means effective to asynchronously read a data element from the external device; and

a write controlling means coupled to the device processing means effective to asynchronously acknowledge the asynchronous read, wherein the device processing means is bypassed during both the asynchronous read and the asynchronous acknowledgment of the asynchronous read.